REMARKS

Claims 1-20 are pending. By this Amendment, Claims 1-8, 10-14, 16-17, and 19-20 are amended, and Claim 18 is canceled without prejudice or disclaimer. Applicant respectfully submits no new material is presented herein.

Allowed/Allowable Claims

Applicant respectfully acknowledges and appreciates the indication by the Examiner that Claims 3-8, 10-14, and 17, although objected to for being dependent upon a rejected base claim, would be allowable if rewritten in independent form, including all of the features of the base claim and any intervening claims.

Claims Rejected—35 U.S.C. § 112

Claims 15 and 16 are rejected under 35 U.S.C. § 112, second paragraph. While Applicant respectfully traverses the rejection because Claims 15 and 16 do not recite dummy memory cells and memory cells having the same circuits, as asserted by the Office Action, the rejection is rendered moot in light of the amendments to Claim 1. Accordingly, Applicant respectfully requests withdrawal of the rejection.

Claims Rejected—35 U.S.C. § 102

Claims 1, 2, and 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,268,869 to Ferris, et al. ("Ferris '869"). Applicant respectfully traverses the rejection.

Claim 1 discloses a semiconductor memory device including, among other features, a memory cell array having a plurality of dummy bit line pairs adjacently disposed to each other, a plurality of bit line pairs adjacently disposed to each other,

dummy memory cells being connected to said dummy bit line pairs respectively, and memory cells being connected to said bit line pairs respectively.

Ferris '869 discloses a memory device having a plurality of memory cells 2 arranged in rows and columns, the cells in each row being connected to a common wordline 4 and the cells in each column being connected between a pair of bit lines 6 and 8. A column of dummy cells 22 is provided among the plurality of memory cells 2 and is connected to a dummy bit line 18, which supplies an input to a timing circuit 16. The dummy memory cells 22 are also connected to a dummy bit line 18a, adjacent to the dummy bit line 18.

However, Ferris '869 does not disclose a memory cell array having a plurality of dummy memory bit line pairs, as recited in Claim 1. Ferris '869 discloses only a single pair of dummy bit lines, as illustrated in Figure 3 of Ferris '869.

The use of the plurality of dummy bit line pairs recited in Claim 1 allows the memory device to control the driving timing of the memory cell by detecting the influence of a process variation in multiple positions in the memory cell array. *See* page 21, lines 1-5 of the written specification. As a result, the influence created by the process variation due to the operation of the semiconductor memory device is alleviated by the plurality of dummy bit line pairs, in contrast to memory devices using only a single dummy bit line pair. *See* page 21, lines 6-10 of the written specification. Therefore, Ferris '869 cannot detect or alleviate the influences of the process variation at a plurality of positions in the memory cell array or control the timing of the driving operation of the memory device.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) and M.P.E.P. § 2131.

As explained above, Ferris '869 does not disclose or suggest each and every feature recited in Claim 1. Therefore, Applicant respectfully submits Claim 1 is not anticipated by, or rendered obvious in view of, Ferris '869 and should be deemed allowable.

Claims 2 and 20 depend from Claim 1. Therefore, Applicant respectfully submits Claims 2 and 20 should be deemed allowable for the same reasons Claim 1 is allowable, as well as for the additional subject matter respectively recited therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Claims Rejected—35 U.S.C. § 103

Claims 9, 18, and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ferris '869 in view of U.S. Patent No. 5,886,939 to Choi, et al. ("Choi '939").

As explained above, Claim 18 is canceled without prejudice or disclaimer. Therefore, the rejection of Claim 18 is rendered moot. Claims 9 and 19 depend from Claim 1 and, therefore, incorporate every feature recited therein. Claim 1 is described above.

Choi '939 discloses a semiconductor memory device having a plurality of sub memory arrays 300, each of which includes a plurality of sub word lines WL0-WLn arranged vertically between sub word line driver regions 500 and sub dummy word lines

DWL arranged at outermost sides of the sum memory cell array. The sub memory arrays 300 further include a plurality of bit lines BL0-BLm intersecting the sub word lines WL0-WLn and a sub dummy bit line pair DBL0/DBLB0 interposed between a sub normal bit line pair BL0/BLB0 and the sub word line driver region 500.

However, contrary to the Office Action's assertion, Choi '939 does not teach or suggest a memory cell array having a plurality of dummy bit line pairs. As illustrated in Figure 5 of Choi '939, the sub memory cell array includes only a single sub dummy bit line pair DBL0/DBLB0. Further, in column 3, lines 56-58 and column 3, line 6 through column 4, line 5, Choi '939 refers only to a single sub dummy bit line pair.

To establish *prima facie* obviousness, each feature of the rejected claim must be taught or suggested by the prior art of record. *See* M.P.E.P. § 2143.03. Because Choi '939 does not disclose or suggest each and every feature recited in Claim 1 and, hence, Claims 8 and 19, Applicant respectfully submits the Office Action has failed to establish *prima facie* obviousness. Therefore, Applicant respectfully submits that Claims 8 and 19 should be deemed allowable for the same reasons Claim 1 is allowable, as well as for the additional subject matter recited respectively therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of Claims 1-17 and 19-20, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108390-00057**.

Respectfully submitted,
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